**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA**
**KAKINADA – 533 003, Andhra Pradesh, India**
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

| II Year – II Semester | | L | T | P | C |
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| DIGITAL IC DESIGN | | | | | |

**OBJECTIVES**

The main objectives of this course are:

• Introduction of digital logic families and inter facing concepts for digital design is considered.

• VHDL fundamentals were discussed to modeling the digital system design blocks.

• Design and implementation of combinational and sequential digital logic circuits is explained.

**Outcomes:**

At the end of this course the student can able to:

• Understand the structure of commercially available digital integrated circuit families.

• Learn the IEEE Standard 1076 Hardware Description Language (VHDL).

• Model complex digital systems at several levels of abstractions, behavioral, structural, and rapid system prototyping.

• Analyze and design basic digital circuits with combinatorial and sequential logic circuits using VHDL.

**UNIT-I**

**Hardware Description Languages.**

**VHDL:** Introduction to VHDL, entity declaration, architecture, data-flow, behavioral and structural style ofmodelings,datatypes,dataobjects,configurationdeclaration,package,generic,operatorsandidentifiers,PROCESS,IF, CASE & LOOPstatements, VHDL libraries.

**Verilog HDL:** Introduction to Verilog HDL, data types, data operators,module statement, wire statement, if-elsestatement, case-endcasestatement,Verilog syntax and semantics(qualitative approach)

**UNIT-II**

**Combinational Logic Design:** Parallel binary adder, carry look ahead adder, BCD adder, Multiplexers anddemultiplexers and their use in combinational logic design, ALU, digital comparators, parity generators, codeconverters, priority encoders. (Qualitative approach of designing and modeling the mentioned combinationallogiccircuits with relevant digital ICs using HDL)

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**UNIT-III**

**Sequential Logic Design:** Registers, applications of shift registers, ripple or a synchronous counters, synchronous counters, synchronous and a synchronous sequential circuits, hazards in sequential circuits. (Qualitative approach of designing and modeling the mentioned sequential logic circuits with relevant digital ICs using HDL)

**UNIT-IV**

**Combinational MOS Logic Circuits**: Introduction, MOS logic circuits with depletion nMOS loads: two-inputNOR gate, generalized NOR structure with multiple inputs, transient analysis of NOR gate, two-input NANDgate, generalized NAND structure with multiple inputs, transient analysis of NAND gate, CMOS logic circuits:CMOS NOR2 gate, CMOS NAND2 gate,complex logic circuits, complex CMOS logic gates, AOI and OAIgates, Pseudo-nMOS gates, CMOS full-adder circuit,CMOS transmission gates (Pass Gates), complementarypass-transistorlogic.

**UNIT-V**

**Sequential MOS Logic Circuits:** Introduction, behavior bistable elements, SR latch circuit, clocked latch andflip-flop circuits: clocked SR latch, clocked JK latch, master-slave flip-flop, CMOS D-latch and Edge-triggeredflip-flop,Schmitt trigger circuit, basic principlesof pass transistor circuits.

**TEXTBOOKS**

1. Modern Digital Electronics–R.P.Jain-Fourth Edition–Tata McGraw Hill Education Private Limited, 2010.
2. CMOS Digital Integrated Circuits-Analysis and Design–Sung-MoKang & Yusuf Leblebici-Tata McGraw Hill Publishing Company Limited, 2006.
3. VHDL/VerilogPrimer - J.Bhasker, Pearson Education/PHI, 3rd Edition.

**REFERENCES**

1. Digital Design Principles & Practices-John F.Wakerly, PHI/Pearson Education Asia, 3rd Edition, 2005.
2. Fundamentals of Digital Logic with VHDL Design - Stephen Brown, Zvonko Vranesic, McGraw Hill, 3rd Edition.